Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of claims:

Claim 1 (currently amended): An integrated circuit, comprising:

a data processing unit;

a buffer memory having registers for storing data for said data processing unit, said buffer memory connected to said data processing unit; and

a setting memory connected to said buffer memory, said setting memory having at least one electrical fuse being at least one of written to and read from through said buffer memory;

said setting memory being only accessible via said registers of said buffer memory, said buffer memory being used as latches for reading out and writing into said setting memory.

Claim 2 (original): The integrated circuit according to claim 1, including circuit elements, said setting memory activating said circuit elements.

Claim 3 (original): The integrated circuit according to claim 2, including a memory having memory areas, said circuit elements being memory elements used to replace at least one of said memory areas.

Claim 4 (previously presented): The integrated circuit according to claim 1, wherein said data processing unit has an arithmetic logic unit.

Claim 5 (original): The integrated circuit according to claim 4, wherein

a register of said registers processes data; and

another register of said registers processes coded instructions for said arithmetic logic unit.

Claim 6 (original): The integrated circuit according to claim 5, wherein said buffer memory is two buffer memories each containing data to be processed.

Claim 7 (original): The integrated circuit according to claim 1, wherein said buffer memory is a latch.

Claim 8 (original): The integrated circuit according to claim 1, wherein said buffer memory has a shift register.

Claim 9 (previously presented): The integrated circuit according to claim 8, wherein said shift register has at least one switch subdividing said shift register into registers for said data processing unit.

Claim 10 (previously presented): The integrated circuit according to claim 1, wherein said data processing unit serially writes to and reads from each of said registers.

Claim 11 (canceled).

Claim 12 (currently amended): A method for determining setting data for a setting memory from address data, stored in a register, of memory areas of a memory that have been identified as defective depending on instruction data stored in a register, which comprises:

providing an integrated circuit having:

a data processing unit;

a buffer memory having registers; and

a setting memory having electrical fuses;

storing data for the data processing unit in the registers of the buffer memory;

connecting the buffer memory to the data processing unit;

connecting the setting memory to the buffer memory, the setting memory being only accessible via the registers of the buffer memory, the buffer memory being used as latches for reading out and writing into the setting memory; and

at least one of writing to and reading from the setting memory through the buffer memory.

Claim 13 (original): The method according to claim 12, which further comprises activating circuit elements with the setting memory.

Claim 14 (original): The method according to claim 13, wherein the circuit elements are memory elements of a memory and which further comprises replacing at least one of the memory areas with the memory elements.

Claim 15 (previously presented): The method according to claim 12, wherein the data processing unit has an arithmetic logic unit.

Claim 16 (original): The method according to claim 15, which further comprises:

processing data with a register; and

processing coded instructions for the arithmetic logic unit with another register.

Claim 17 (original): The method according to claim 16, wherein the buffer memory is two buffer memories each containing data to be processed.

Claim 18 (original): The method according to claim 12, wherein the buffer memory is a latch.

Claim 19 (original): The method according to claim 12, wherein said buffer memory has a shift register.

Claim 20 (original): The method according to claim 19, which further comprises subdividing the shift register into

registers for the processing unit with at least one switch of the shift register.

Claim 21 (original): The method according to claim 12, which further comprises serially writing to and reading from each of the registers with the processing unit.

Claim 22 (canceled).

Claim 23 (new). An integrated circuit, comprising:

a data processing unit;

a buffer memory having registers for storing data for said data processing unit, said buffer memory connected to said data processing unit; and

a setting memory connected to said buffer memory, said setting memory having at least one electrical fuse being at least one of written to and read from through said buffer memory;

said buffer memory having a shift register, said shift register having at least one switch subdividing said shift register into said registers for said data processing unit.